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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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James R Duzan
Trask Britt & Rossa
P O Box 2550
Salt Lake City, UT 84110

EXAMINER

KANG, DONGHEE

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/543,034

Applicant(s)

JIANG, TONGBI

Examiner

Donghee Kang

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4-9 and 11-15 is/are rejected.
- 7) ☒ Claim(s) 2-3 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 5 April 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Continuing Domestic Data

1. Acknowledgment is made that this application is a divisional of application serial No. 09/223,059, filed 30 December 1998, which issued as U.S. Patent No. 6,655,354.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 24, 2002 has been entered.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the phrase "*an encapsulant material encasing.... said glob top material*" in claim 8 must be shown in Fig.6 or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims **1, 4-5, 7 & 9** are rejected under 35 U.S.C. 102(e) as being anticipated by Yew et al. (US 6,049,129).

Regarding claim **1**, Yew et al. disclose a semiconductor die assembly comprising (Figs. 4&5 and Col.8, lines 45 – Col.9, line7):

a printed circuit board (70; Col.8, lines 51-52) having a first surface (94) and a second surface (92), wherein said printed circuit board includes at least one opening (86; Col.8, line 62) defined therethrough between said printed circuit board first surface (94) and said printed circuit board second surface (92), wherein the printed circuit board is constructed from a material such as FR-4 (Col.3, lines 58-60 & Col.8, lines 53-54);

at least one semiconductor chip (50) having an active surface with at least one electrical connection area (120; Col.8, lines 59-60) disposed on said semiconductor chip active surface, said at least one semiconductor chip oriented having said at least one electrical connection area (120) substantially aligned with said at least one printed circuit board opening (86); and

at least one adhesive tape (60; Col.8, lines 47-50) interposed between and attaching said semiconductor chip active surface and said printed circuit board first surface (94), wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor chip to an edge of said at least one printed circuit board opening.

The use of the phrase "semiconductor chip" and "semiconductor die" are considered to be interchangeable in the art. Thus, the "semiconductor chip" would meet the claimed phrase "semiconductor die".

The phrase "printed circuit board" would meet the claimed phrase "semiconductor substrate" because applicant noted that "the semiconductor substrate" can be an FR-4 printed circuit board (see disclosure; lines 11-12 on page 13).

Therefore, the 102 (e) rejection anticipates each and every element as set forth in claim 1.

Regarding claim 4, Yew et al. disclose the semiconductor chip assembly further including at least one electrical connection (80) extending between said at least one electrical connection area (120) and at least strips (82) on said printed circuit board second surface (Col.8, lines 60-62). The phrase "strips" would meet the claimed phrase "trace" because the phrases, strips and trace, are often used interchangeable in the art.

Regarding claim 5, Yew et al. disclose the at least one electrical connection comprises a bond wire (Col.8, lines 60-62).

Regarding claim 7, Yew et al. disclose the semiconductor chip assembly further including a potting material (90) disposed within said at least one printed circuit board

opening encasing said at least one electrical connection, wherein the potting material comprises epoxies or silicone (Col.7, lines 26-34 & Col.8, lines 65-66). The "potting material" would meet the claimed phrase "glob top material" because the phrase, potting material and glob top material, are often used interchangeable in the art, and the potting material and glob top material both include epoxy or silicone (see disclosure; lines 18-20 on page 2).

Regarding claim 9, Yew et al. disclose the at least one adhesive tape (60) comprises a planar carrier film (polyimide) including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon (Col.3, lines 53-54).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al.

Yew et al disclose a semiconductor die assembly, comprising (Figs. 4&5 & Col.8, lines 45 – Col.9, line7):

a printed circuit board (70; Col.8, lines 51-52) having a first surface (94) and a second surface (92), wherein said printed circuit board includes at least one opening

(86; Col.8, line 62) defined therethrough between said printed circuit board first surface (94) and said printed circuit board second surface (92);

at least one semiconductor chip (50) having an active surface with at least one electrical connection area (120; Col.8, lines 59-60) disposed on said semiconductor chip active surface, said at least one semiconductor chip oriented having said at least one electrical connection area (120) substantially aligned with said at least one printed circuit board opening (86); and

at least one adhesive tape (60; Col.8, lines 47-50) interposed between and attaching said semiconductor chip active surface and said printed circuit board first surface (94), wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor chip to an edge of said at least one printed circuit board opening.

The use of the phrase "semiconductor chip" and "semiconductor die" are considered to be interchangeable in the art. Thus, the "semiconductor chip" would meet the claimed phrase "semiconductor die".

The phrase "printed circuit board" would meet the claimed phrase "semiconductor substrate" because applicant noted that "the semiconductor substrate" can be an FR-4 printed circuit board (see disclosure; lines 11-12 on page 13).

Yew et al. do not expressly teach that the semiconductor chip assembly is incorporated into a computer system. However, Yew et al. teach that the semiconductor chip (50) can be an integrated circuit component such as a DRAM, an EPROM or a SRAM (Col.3, lines 49-51). It is well known in the art that the computer system includes

the memory chips, such as DRAM, EPROM, or SRAM. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory chips, such as DRAM, EPROM, or SRAM of Yew et al. into the computer system since the computer system is required to have a storage area to save information.

8. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of APA (Fig.15) and Khandros et al. (US 5,148,266).

Yew et al. do not expressly teach the electrical connection comprising a Tape Automate Bonding (TAB) connection. Khandros et al. note that the most widely utilized primary interconnection methods are wire bonding, tape automated bonding (TAB) and flip-chip bonding (Col.2, lines 23-25). Tape automated bonding (TAB) can provide the assembly with good resistance to thermal stresses (Col.3, lines 6-8). APA in Fig.15 also teaches a TAB connector (216) attached to bond pad (208) on the semiconductor chip and trace (212) on the semiconductor substrate. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the bond wire of Yew et al. with tape automated bonding (TAB) as taught by APA and Khandros since the tape automated bonding (TAB) can provide the semiconductor chip assembly with good resistance to thermal stresses.

9. Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of Murakami et al. (US 5,612,569).

Yew et al. teach the semiconductor chip assembly further including an encapsulant material (90) encasing the back of semiconductor chip (50) (Col.7, lines 21-34 & Col.9, lines 2-3) but do not teach the encapsulant material encasing said glob top (potting) material and the principal surface of the semiconductor chip. However, Murakami et al. in Fig.34 teach the semiconductor chip having its principal surface covered with a glob top material (20) which is more flexible or fluid than the mold resin (2A) to cover the bonding wires while the outside being sealed up with a resin. Note that the circuit in the integrated package must be sealed to isolate it from the atmosphere, dirt, moisture, and other contamination which could destroy the circuit or affect its operation. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mold the outside of the glob top (potting) material with a resin (encapsulant material) as taught by Murakami et al. in the Yew et al.'s device in order to protect the semiconductor package from contaminations.

10. Claims **11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of Boyko et al. (US 5,784,782).

Regarding claims **12 & 13**, Yew et al. teach substantially the entire claimed structure, as applied to claim 1 explained above, except that the semiconductor chip assembly further comprising at least one fillet located proximate said at least one adhesive tape, said edge of said at least one semiconductor substrate opening, and said active surface of said at least one semiconductor die.

Applicant noted that filleting of the adhesive layers is caused by flow of the material in the adhesive layers during attachment of the semiconductor die to the semiconductor substrate by processing known in the art, such as heating processes, which cause the adhesive layers to momentarily flow out from the space between the carrier film and the semiconductor substrate and thereafter solidify (see disclosure; lines 18-23 on page 16).

Yew et al. also teach that the attachment of the semiconductor die (50) to the semiconductor substrate (70) is conducted under pressing and heating process (Col.4, lines 32-25). This pressing and heating process would cause the adhesive film to flow to and slightly within the base perimeter of the opening (86) and would form fillets located proximate the adhesive film, the printed circuit opening, and active surface of the semiconductor chip because the adhesiveness of the tape would stick to the surface of semiconductor die.

Even if this is not true, Boyko et al. (Fig.5 & Col.4, lines 32-42) teach that the heat and pressure cause the sticker sheet to bind ground plate to metallized dielectric layer (22) and cause the sticker sheet material to flow to and slightly within the base perimeter of the cavity (31). This leaves a fillet (82) of the sticker sheet material along the bottom perimeter of the cavity. This fillet has a smooth concave surface which minimizes stress concentrations and the tendency to trap fluids or contaminants during subsequent processing.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form incorporate fillets of Boyko et al. into the Yew et al.'s device

Art Unit: 2811

located proximate the adhesive film, the printed circuit opening, and active surface of the semiconductor chip since it minimizes stress concentrations and the tendency to trap fluids or contaminants during subsequent processing.

Regarding claims **11 & 14**, Yew et al. teach substantially the entire claimed structure, as applied to claim 1 explained above, except that the semiconductor chip assembly further comprising at least one fillet located proximate said at least one adhesive tape, said edge of said at least one semiconductor chip, and said semiconductor substrate first surface.

Applicant noted that filleting of the adhesive layers is caused by flow of the material in the adhesive layers during attachment of the semiconductor die to the semiconductor substrate by processing known in the art, such as heating processes, which cause the adhesive layers to momentarily flow out from the space between the carrier film and the semiconductor substrate and thereafter solidify (see disclosure; lines 18-23 on page 16).

Yew et al. also teach that the attachment of the semiconductor die (50) to the semiconductor substrate (70) is conducted under pressing and heating process (Col.4, lines 32-25). This pressing and heating process would cause the adhesive film to flow to said edge of said at least one semiconductor chip and would form fillets located proximate the adhesive film, said edge of said at least one semiconductor chip, and said semiconductor substrate first surface because the adhesiveness of the tape would stick to the surface of semiconductor die.

Even if this is not true, Boyko et al. teach that the heat and pressure cause the sticker sheet to bind ground plate to metallized dielectric layer 22 and cause the sticker sheet material to flow to and slightly within the base perimeter of the cavity 31. This leaves a fillet 82 of the sticker sheet material along the bottom perimeter of the cavity. This fillet has a smooth concave surface which minimizes stress concentrations and the tendency to trap fluids or contaminants during subsequent processing. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form fillets located proximate said at least one adhesive tape, said edge of said at least one semiconductor chip, and said semiconductor substrate first surface in the Yew et al.'s device since it minimizes stress concentrations and the tendency to trap fluids or contaminants during subsequent processing.

Allowable Subject Matter

11. Claims **2-3 & 10** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Yew et al. fail to teach or suggest the width of adhesive tape extends beyond the edge of the semiconductor substrate opening and edge of the semiconductor die. It is desirable to improve the ability to visually inspect for proper attachment of the semiconductor chip to the semiconductor substrate.

Art Unit: 2811

Yew et al. fail to teach or suggest a composition of the first adhesive differs from a composition of the second adhesive. The use of differing adhesives compensates for the disparity in thermal expansion values typically existing between semiconductor substrate and semiconductor chip. Accordingly, one of ordinary skill in the art would not have been motivated to modify the teaching of Yew et al. to meet the claimed limitation.

Response to Arguments

12. Applicant's arguments with respect to claims 1, 4-9 and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Donghee Kang
Examiner
Art Unit 2811

dhk
December 16, 2002